University of Victoria | Graduate Studies

Notice of the Final Oral Examination
for the Degree of Master of Arts

of

MISCHA FISHER

BA (University of Victoria, 2007)

"CPU Product Line Lifecycles: Econometric Duration Analysis using Parametric and Non-Parametric Estimators"

Department of Economics

Friday, March 2, 2018
10:30 A.M.
Business and Economics Building
Room 371

Supervisory Committee:
Dr. Kenneth Stewart, Department of Economics, University of Victoria (Supervisor)
Dr. David Giles, Department of Economics, UVic (Member)

External Examiner:
Dr. Mary Lesperance, Department of Mathematics and Statistics, UVic

Chair of Oral Examination:
Dr. Gregory Rowe, Department of Greek and Roman Studies, UVic

Dr. Stephen V. Evans, Acting Dean, Faculty of Graduate Studies

Abstract

This thesis provides a comprehensive history of the statistical background and uses of survival analysis, and then applies econometric duration analysis to examine the lifecycles of product lines within the microprocessor industry. Using data from Stanford University's CPUDB, covering Intel and AMD processors introduced between 1971 and 2014, the duration analysis uses both parametric and nonparametric estimators to construct survival and hazard functions for estimated product line lifetimes within microprocessor product families. The well-known and widely applied non-parametric Kaplan-Meier estimator is applied on both the entire sample as a whole, and segmented estimate that considers product line lifecycles of Intel and AMD separately, with median survival time of 456 days. The parametric duration analysis uses both the semiparametric Cox proportional hazard model, and the fully parametric accelerated failure time model across the Weibull, Exponential and Log-Logistic distributions, which find modest association between higher clock speed and transistor count on diminishing expected time in the marketplace for microprocessors, while the number of cores and other attributes have no predictive power over expected survival times. It is expected that the transistor count and clock speed of a given processor’s negative effect on expected duration, likely captures the co-trending of growth in transistor count with a larger marketplace and broader product categories.